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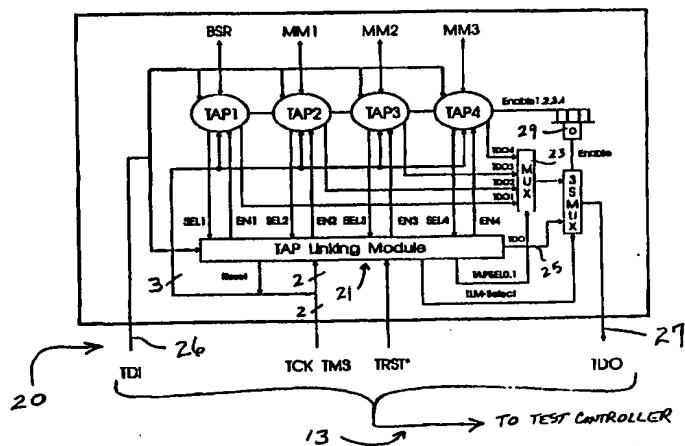
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(54) Method and device for testing integrated circuits

(57) A TAP linking module (21, 51) permits plural TAPs (TAPs 1-4) to be controlled and accessed from a

test bus (13) via a single TAP interface (20).

Figure 2



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Description

FIELD OF THE INVENTION

The invention relates generally to evaluation of the functionality of electronic integrated circuits and, more particularly, to improvements in the control and design of test access ports (TAPs) within integrated circuits.

BACKGROUND OF THE INVENTION

The IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE STD 1149.1) is a well known IEEE test standard that provides scan access to scan registers within integrated circuits (ICs). Figure 12 shows a schematic of the 1149.1 test logic. The test logic comprises a TAP controller 120, an instruction register, and plural test data registers. The TAP controller 120 is connected to test mode select (TMS), test clock (TCK), and test reset (TRST*) pins. The TAP controller 120 responds to control input on TCK and TMS to scan data through either the instruction or data registers, via the test data input (TDI) and test data output (TDO) pins. TRST* is an optional pin used to reset or initialize the test logic, (i.e. TAP controller, instruction register, and data registers). The inputs to the instruction and data registers are both directly connected to the TDI input pin. The output of the instruction and data registers are multiplexed to the TDO pin. During instruction register scans, the TAP controller 120 causes the multiplexer 121 to output the instruction register on TDO. During data register scans, the TAP controller 120 causes the multiplexer 121 to output the data register on TDO. The instruction scanned into the instruction register selects which one of the plural data registers will be scanned during a subsequent data register scan operation. When the TAP controller 120 is scanning data through the instruction or data registers, it outputs control to enable the output stage to output data from the TDO pin, otherwise the TAP controller disables the output stage.

Figure 13 shows how four ICs, each IC including the TAP controller 120, instruction register, and data registers of Figure 12, would be connected at the board level for serial data transfer (TDI, TDO) and parallel control (TMS, TCK).

Figure 14 shows the state diagram operation of the Figure 12 TAP controller. The TAP controller 120 is clocked by TCK and responds to TMS input to transition between its states. The logic state of TMS is shown beside the paths connecting the states of Figure 14. The Test Logic Reset state is where the TAP controller 120 goes to in response to a power up reset signal, a low on TRST*, or an appropriate TMS input sequence. From Test Logic Reset the TAP controller 120 can transition to the Run Test/Idle state. From the Run Test/Idle state the TAP controller 120 can transition to the Select DR Scan state. From the Select DR Scan state, the TAP

controller 120 can transition into a data register scan operation or to the Select IR scan state. If the transition is to the data register scan operation, the TAP controller 120 transitions through a Capture DR state to load parallel data into a selected data register, then shifts the selected data register from TDI to TDO during the Shift DR state. The data register shift operation can be paused by transitioning to the Pause DR state via the Exit1 DR state, and resumed by returning to the Shift DR state via the Exit2 DR state. At the end of the data register shift operation, the TAP controller 120 transitions through the Update DR state to update (output) new parallel data from the data register and thereby complete the data register scan operation. From the Update DR state, the TAP controller 120 can transition to the Run Test/Idle state or to the Select DR Scan state.

If the Select IR Scan state is entered from the Select DR Scan state, the TAP controller 120 can transition to the Test Logic Reset state or transition into an instruction register scan operation. If the transition is to an instruction register scan operation, Capture IR, Shift IR, optional Pause IR, and Update IR states are provided analogously to the states of the data register scan operation. Next state transitions from the Update IR state can be either the Run Test/Idle state or Select DR Scan state. If the TAP controller 120 transitions from the Select IR Scan state into the Test Logic Reset state, the TAP controller 120 will output a reset signal to reset or initialize the instruction and data registers.

Figure 15 shows that state transitions of the Figure 12 TAP controller 120 occur on the rising edge of the TCK and that actions can occur on either the rising or falling edge of TCK while the TAP controller 120 is in a given state.

The term TAP referred to hereafter will be understood to comprise a TAP controller, an instruction register, test data registers, and TDO muxing of the general type shown in Figure 12, but differing from Figure 12 according to novel features of the present invention described with particularity herein. The 1149.1 standard was developed with the understanding that there would be only one TAP per IC. Today, ICs may contain multiple TAPs. The reason for this is that ICs are being designed using embedded megamodule cores which contain their own TAPs. A megamodule is a complete circuit function, such as a DSP, that has its own TAP and can be used as a subcircuit within an IC or as a standalone IC. An IC that contains multiple megamodules therefore has multiple TAPs.

In example Figure 1, an IC 10 containing four TAPs is shown. TAP1 is shown connected to the boundary scan register (BSR) to provide the 1149.1 standard's conventional board level interconnect test capability. TAP1 can also be connected to other circuitry within the IC that exists outside the megamodules. TAP2 is an integral part of megamodule MM1. Likewise TAP3 and TAP4 are integral parts of megamodules MM2 and

MM3. Each TAP of Figure 1 includes a conventional 1149.1 TAP interface 11 for transfer of control (TMS, TCK and TRST) and data (TDI and TDO) signals. However, the 1149.1 standard is designed for only one TAP to be included inside an IC, and for the 1149.1 TAP interface of this one TAP to be accessible externally of the IC at terminals (or pins) of the IC for connection via 1149.1 test bus 13 to an external test

It is therefore desirable controller to provide an architecture wherein all TAPs of an IC can be controlled and accessed from an external 1149.1 test bus via a single externally accessible 1149.1 TAP interface. The present invention provides an architecture which permits plural TAPs to be selectively accessed and controlled from a single 1149.1 TAP interface. The invention further provides access to a single register via any selected one of a plurality of TAPs. The invention further provides a TAP controller whose state machine control can be selectively overridden by an externally generated override signal which drives the state machine synchronously to a desired state. The invention further provides a TAP instruction which is decodable to select an external data path. Also according to the invention, sequential access of TAPs from a single 1149.1 TAP interface permits test operations associated with different TAPs to timewise overlap each other.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described, by way of example, with reference to the accompanying drawing in which:-

Figure 1 illustrates a test controller connected to an integrated circuit having multiple TAPs therein;

Figure 2 illustrates an integrated circuit having multiple TAPs therein according to the present invention;

Figure 3 illustrates the TAP Linking Module of Figure 2 in greater detail;

Figure 4 illustrates the TLM TAP Controller of Figure 3 in greater detail;

Figure 5 illustrates another exemplary integrated circuit having multiple TAPs therein according to the present invention;

Figure 6 illustrates in greater detail the TAP Linking Module of Figure 5;

Figure 7 illustrates TAP4 of Figures 2 and 5 in greater detail;

Figure 8 illustrates multiplexing circuitry associated with the scan input of TAP4 of Figure 5;

Figure 9 shows a state diagram associated with the TAP controller of Figure 7;

Figure 9A illustrates in more detail a portion of the TAP controller of Figure 7;

Figures 10-11 are timing diagrams which illustrate examples of how the TAPs of Figures 2 and 5 can be synchronously linked to and unlinked from the test bus of Figures 2 and 5;

Figure 12 illustrates the architecture of a conventional 1149.1 TAP;

Figure 13 illustrates a plurality of integrated circuits connected in a conventional manner for 1149.1 testing;

Figure 14 is a state diagram associated with the conventional TAP controller of Figure 12;

Figure 15 is a timing diagram which illustrates when state changes and other actions can occur in the conventional TAP architecture of Figure 12;

Figure 16 illustrates in greater detail a portion of prior art Figure 12;

Figure 16A illustrates conventional instructions associated with the architecture of Figure 16;

Figure 17 illustrates in greater detail a portion of TAP4 from Figure 7; and

Figure 17A illustrates a set of instruction pairs associated with the architecture of Figure 17.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2 shows an exemplary IC according to the invention, including a TAP Linking Module (TLM) 21 which is coupled to each TAP via select (SEL1-4) and enable (EN1-4) signals, and to an externally accessible 1149.1 interface 20 including TDI, TCK, TMS, TRST*, and TDO pins. The TAPs are connected to the TCK and TMS pins and to the Reset output from the TLM. The SEL1-4 signals are outputs from the TAPs to the TLM, and the EN1-4 signals are output from the TLM to the TAPs. Each TAP's select signal is output in response to a special instruction scanned into its instruction register. The instruction sets the select output from the TAP high, which causes the TLM to be selected as the data register scan path between the IC's TDI and TDO pins 26 and 27. A conventional data register scan operation is used to capture data into and then shift data through the TLM from TDI to TDO. During such a TLM scan operation, the TLM Select output signal from TLM makes a connection from the TLM's TDO output 25 to the IC's connection

TDO output 27, via the multiplexer 3SMUX. Also during a TLM scan operation, an Enable output from the currently enabled TAP (one of Enable 1,2,3,4) enables a TDO output buffer (in 3SMUX) via OR gate 29. This is analogous to enabling the output stage in Figure 12. Following the TLM scan operation, TLM outputs EN1-4 signals to the TAPs and TAPSEL0-1 signals to the multiplexer 23 to establish a TAP link configuration. The data scanned into the TLM selects one of the four outputs EN1-4 to be active to enable the corresponding one of the TAPs. Also the TAPSEL0-1 and TLM-Select signals will cause the TDO of the enabled TAP (one of TDO1-TDO4) to be connected to the IC's TDO pin 27.

From this description it is seen that the TLM 21 operates to selectively enable one of the TAPs to be accessed via the IC's 1149.1 test pins. The circuit coupled to the enabled TAP (BSR, MM1, MM2, MM3) can therefore be accessed directly from the 1149.1 test pins. A presently enabled TAP can select and scan the TLM 21 which in turn will select and enable another TAP. When another TAP is enabled, the previously enabled TAP is disabled and remains so until it is enabled again by the TLM. The EN1-4 inputs to the TAPs can enable or disable the TAPs in many ways. For example, the EN1-4 inputs could simply be used to gate TCK "ON" and "OFF". Alternatively and preferably, the EN1-4 inputs could be included in the designs of the TAP controller state machines to keep the TAP in its Run-Test/Idle state when disabled. This preferred method of using the EN1-4 signals is described below in connection with Figures 9 and 9A.

Figure 3 shows one circuit example implementation of TLM 21. The circuit comprises a TLM TAP controller 31, a 2-bit shift register, decode logic, and a link update register. The TLM TAP controller 31 is always enabled to follow the test bus protocol on the TCK and TMS pins, (i.e. the TLM TAP controller is always synchronized to the state of the 1149.1 test bus 13 connected to the TCK and TMS pins). However, the outputs of the TLM TAP controller (i.e. TLM-ShiftDR, TLM-ClockDR, TLM-UpdateDR, and TLM-Select) are only enabled during a data register scan operation and only if the select input (SEL1-4) from the currently enabled TAP is high.

If the currently enabled TAP inputs a high select input at one of SEL1-4, the TLM TAP controller 31 will respond to TCK and TMS to output control on TLM-ShiftDR, TLM-ClockDR, and TLM-Select to capture and shift data through the 2-bit shift register, and then output TLM-UpdateDR control to update the decoded output from the shift register to the link update register. This capture, shift, and update operation is a well known TAP controller scan operation taught in IEEE STD 1149.1 and shown in Figures 5-1 and 5-7 thereof. During this scan operation, the TLM TAP controller outputs TLM-Select control to couple the TDO output of TLM 21 to the IC's TDO pin 27, via the 3SMUX of Figure 2. Also during the scan operation, the output of the 3SMUX is activated by the enabled TAP (one of Enable1-4) to out-

put data on the IC's TDO pin 27. The data from the link update register is output as EN1-4 and TAPSEL0-1 to enable the desired TAP and its TDO connection (one of TDO1-4) to the IC's TDO pin 27. The active one of enable signals EN1-4 qualifies a corresponding one of select signals SEL1-4 at one of AND gates 33-36, whereby the corresponding one of SEL1-4 can be input to the TLM TAP controller via the OR gate 37. Select signals from disabled TAPs are gated "OFF" by the AND gates associated with the inactive ones of enable signals EN1-4. The decode from the 2-bit shift register allows each of TAP1, TAP2, TAP3, or TAP4 to be individually selected, accessed, controlled and scanned from the 1149.1 pins at 20.

Exemplary Figure 4 shows a detail view of the TLM TAP controller 31. The TLM TAP controller comprises the conventional 1149.1 TAP controller 120 of Figure 12 and gating to enable or disable the TLM-Select, TLM-ClockDR, TLM-ShiftDR, and TLM-UpdateDR outputs of the TLM TAP controller. After power up reset, the 1149.1 TAP controller 120 is always synchronized to the state of the 1149.1 test bus. Note that the output signal 39 of the Figure 3 AND gate 38 is connected to 1149.1 TAP controller 120 at input node 123 thereof where the TRST* signal would conventionally be connected (contrast Figure 12). The 1149.1 TAP controller's conventional outputs are gated "OFF" by the OR gates 41 and 43, and AND gates 45 and 47 so that the state of the TLM's shift register and link update register are not disturbed during data register scans occurring while the SEL input from OR gate 37 (Figure 3) is low. TLM-Select and TLM-ClockDR are high while SEL is low, and TLM-UpdateDR and TLM-ShiftDR are low while SEL is low. These output conditions match what the conventional 1149.1 TAP controller 120 would output on the analogous signal types (i.e. Select, ClockDR, ShiftDR, UpdateDR) when data register scans are not being performed. When the SEL input is high, the gated outputs from the TLM TAP controller follow the conventional 1149.1 TAP controller outputs. The Reset output from the TLM TAP controller is always enabled to output the conventional 1149.1 Reset signal to the TAPs within the IC. The TLM TAP controller can be viewed as the master TAP controller in the IC since it has reset authority over all other TAPs.

When the TLM TAP controller is reset (i.e. forced to the Test Logic Reset state of Figure 14) by the power up reset circuit, or by activation of the TRST* pin, or by an appropriate TMS sequence, it outputs a Reset signal. Either the power-up reset circuit or the TRST* signal can drive the output 39 of AND gate 38 (see Figure 3) low and thereby force the Test Logic Reset state. An appropriate sequence of logic 1's on TMS can also put the TLM TAP controller in the Test Logic Reset state (see Figure 14). Internal to the TLM 21, the Reset signal loads the link update register with EN1 and appropriate TAPSEL0-1 control (see Figure 3) to enable and link TAP1 between the TDI pin 26 and 3SMUX (see Figure

2). TLM Select is driven high when controller 31 is in the Test Logic Reset state because the Select output from the conventional 1149.1 TAP controller 120 goes high in the Test Logic Reset state. When TLM Select is high, the output of MUX 23 is connected to TDO pin 27 via 3SMUX. By initially selecting TAP1 to be active, the IC appears to test bus 13 to be operating as would a one-TAP IC described in the 1149.1 standard. Following the initial selection of TAP1, the TLM can be selected by TAP1 and then scanned to select any other TAP in the IC to become the active TAP. External to the TLM 21, the Reset signal initializes all the TAPs to the Test Logic Reset state of Figure 14.

Figure 5 shows another example IC according to the invention, including a TAP Linking Module (TLM 51) which is coupled to TAPs, 1149.1 test pins, and multiplexers similarly to Figure 2. Additionally, the TLM 51 is coupled to the TAPs 2-4 via Link Control (LC2-4) signals. The operation of TLM 51 is similar to TLM 21 of Figure 2, except: (1) the TLM 51 can be loaded with data to enable more than one TAP at a time in the IC; and (2) the TLM 51 outputs link control to the TAPs to allow linking the TAPs together in different arrangements within a single scan path between the TDI 26 and TDO 27 pins. The linking and enabling of multiple selected TAPs permits the circuits associated with the TAPs (BSR, MM1, MM2, MM3) to be accessed at the same time.

In Figure 5 it is seen that TAPs 2-4 have multiple scan inputs. In particular, the TAPs 2-4 have scan inputs as follows: TAP2 has TDI pin 26 and TDO1; TAP3 has TDI pin 26, TDO1 and TDO2; and TAP4 has TDI pin 26, TDO1, TDO2 and TDO3. This is to allow for serially concatenating enabled TAPs together in different ways. For example TAP1 and TAP4 can be enabled at the same time and linked together into the serial path between TDI 26 and TDO 27. In this arrangement, TAP1 and TAP4 can participate together during test while TAP2 and TAP3 are disabled. The Link Control signals LC2-4 to TAPs 2-4 select the appropriate scan input to the TAPs to make a particular serial link between TAPs. TLM 51 can provide the following TAP linking arrangements between TDI 26 and TDO 27:

TAP1 Links: TAP1, TAP1&2, TAP1&3, TAP1&4,
TAP1,2&3, TAP1,2,&4, TAP1,2,3&4,
TAP1,3&4
TAP2 Links: TAP2, TAP2&3, TAP2&4, TAP2,3&4
TAP3 Links: TAP3, TAP3&4
TAP4 Links: TAP4

The more scan inputs per TAP, the more possible linking arrangements. For example, TAP3 could also have TDO4 as a scan input in addition to those shown in Figure 5. The multiplexing circuitry associated with the multiple scan inputs of the Figure 5 TAPs is not shown in Figure 5 for clarity, but an example is described below in relation to Figure 8.

Figure 6 shows one circuit example implementation of the TLM 51. The TLM 51 is similar to the TLM 21 of Figure 3 except: (1) the shift register is longer due to the additional decode required for linking multiple TAPs; (2) the decode circuit and link update register provide additional output for link controls LC2-4; and (3) select inputs from all enabled and linked TAPs will be qualified by the corresponding active enable signals for input to the TLM TAP controller 31 via the AND and OR gates 33-37.

Example Figure 7 shows a portion of the design of TAP4 of Figure 2. The other TAPs of Figure 2 can be analogously designed. The TAP controller 71 includes an input for the EN4 signal from the TLM 21, which is used to enable or disable the TAP controller 71. Also, TAP controller 71 has an input 73 connected to the Reset output from the TLM 21 to provide global reset of all TAPs. The TAP4 instruction register decode includes the SEL4 output to the TLM 21. Also, an instruction is provided to allow setting the SEL4 output high to enable scan access of the TLM 21.

25 Example Figure 8 shows TDI pin 26, TDO1, TDO2 and TDO3 multiplexed onto the scan input of TAP4 to support the design of Figure 5. The scan inputs of the other TAPs of Figure 5 are multiplexed analogously. In this example, a 4:1 multiplexer 81 is connected to the TLM 51 via two link control signals LC4A and LC4B to control which scan input (TDI pin 26, TDO1, TDO2, or TDO3) is connected to the TAP's TDI input .

30 Figure 9 shows an example TAP controller design to support enabling and disabling TAPs 1-4 of Figures 2 and 5 using the EN1-4 outputs from either TLM 21 or TLM 51. The TAP controller state diagram of Figure 9 corresponds to the TAP controller 71 of Figure 7, and includes a Run Test/Idle state wherein the enable signal (in this case EN4) is evaluated along with the TMS signal to determine the next state transition. In the Run Test/Idle state of Figure 9, the next state will always be the Run Test/Idle state if EN4 is low, regardless of the logic level on TMS. If EN4 is high, the next state from Run Test/Idle is determined by the logic level on TMS. In the UpdateDR state the EN4 signal is evaluated along with the TMS signal to determine the next state transition. In the UpdateDR state of Figure 9, the next state will always be Run Test/Idle if EN4 is low, regardless of the logic level on TMS. If EN4 is high, the next state from UpdateDR is determined by the logic level on TMS. Although Figure 9 illustrates an example state diagram for the TAP controller of TAP4, TAPs 1-3 can be analogously designed.

The Run Test/Idle state of Figure 9 provides, in addition to its conventional run test or idle functions, a stable state for the TAP controller to assume and remain in when it is not enabled to be linked to the 1149.1 test bus pins. Using the Run Test/Idle state as the stable state for unlink is advantageous because one well known method of initializing test operations associated with a given instruction is to transition the TAP into Run

Test/Idle with the given instruction in the instruction register. An example of this advantage of using Run Test/Idle as the stable state for unlink is described hereinbelow with respect to the RunBist instruction.

The UpdateDR state of Figure 9 provides, in addition to its conventional data update function, a link change state where a presently enabled TAP controller gets disabled and goes to the Run Test/Idle state while a new TAP controller becomes enabled to follow the ICs test bus pins.

For example, in Figure 2 and after a Reset, the TLM TAP controller 31 and all the TAP controllers of TAPs1-4 will be in the Test Logic Reset state of Figure 9. The IC's 1149.1 test bus pins will also be in Test Logic Reset state as driven by the external test controller. When the test bus moves from Test Logic Reset to Run Test/Idle, all the TAP controllers of TAPs1-4 will follow the test bus. However when the test bus moves from Run Test/Idle to Select DR Scan, only the TAP controller of TAP1 (TAP1 is enabled at reset to be the linked TAP as previously described) will follow. The other TAP controllers of TAPs2-4 will remain in Run Test/Idle because their enable inputs EN2-4 are low. TAP1 will continue following the test bus until another TAP is enabled by scanning the TLM 21. When the TLM 21 is scanned, the new enable and TAPSEL0,1 control will be updated from the TLM 21. For example if TAP2 is the new TAP to be selected, the EN1 for TAP1 will go low and the EN2 for TAP2 will go high in the UpdateDR state. Also, the TAPSEL0,1 outputs will change to output TDO2 from multiplexer 23. When the enable outputs from the TLM 21 change, the TAP controller of TAP1 will see a low on EN1 and it will be forced to transition from the UpdateDR state to the Run Test/Idle regardless of the logic level on TMS. When the TAP controller of TAP2 sees a high on EN2, it will be enabled to either (1) transition from the Run Test/Idle state to the Select DR Scan state if TMS is high, or (2) remain in the Run Test/Idle state if TMS is low. So while a TAP being unlinked is forced to transition from the UpdateDR state to the Run Test/Idle state regardless of the logic level on TMS, a TAP being linked can either stay in the Run Test/Idle state if the next state of the test bus is the Run Test/Idle state (TMS=0), or transition to the Select DR Scan state if the next state of the test bus is the Select DR Scan state (TMS=1).

Figure 9A shows an example of how TAP controller 71 of Figure 7 can use the EN4 signal to realize the state diagram of Figure 9. The TAP state machine circuit 97 of Figure 9A can be the conventional 1149.1 TAP state machine that implements the state diagram of Figure 14. However, the input 95 where TMS is conventionally applied to the state machine is connected in Figure 9A to the output of a multiplexer 90 whose data inputs are TMS and the output 91 of an AND gate 93 whose inputs are TMS and EN4. The multiplexer 90 is controlled to select AND gate output 91 when the decoded state of the TAP state machine is Update DR or Run

Test/Idle, and to otherwise select TMS.

Apart from the improvements associated with Figures 7-9A (and Figure 17 below), TAPs1-4 of Figures 2 and 5 can otherwise conform to the conventional 1149.1 TAP design of Figure 12. In fact, the TAP controller 71 of Figures 7-9A will operate as conventional 1149.1 TAP controller 120 of Figure 12 if EN4 is tied high. Note that input 73 of TAP controller 71 corresponds to the TRST* input of conventional TAP controller 120 (see Figure 12).

The examples in Figures 10 and 11 illustrate two ways a TAP can be synchronously linked to the test bus 13. The Figure 10 example shows how a TAP is synchronously linked to the test bus 13 when the test bus transitions from UpdateDR to Run Test/Idle state. The Figure 11 example shows how a TAP is synchronously linked to the test bus 13 when the test bus transitions from UpdateDR to Select DR Scan.

Figure 10 shows a timing example wherein unlinked TAP2 becomes linked and linked TAP1 becomes unlinked while the test bus transitions from the UpdateDR state to the Run Test/Idle state to the Select DR Scan state. The link change occurs on the falling edge of the TCK in the UpdateDR state with EN1 of TAP1 going low and EN2 of TAP 2 going high. On the next rising TCK edge, the test bus transitions into the Run Test/Idle state, TAP1 (now unlinked) is forced to transition to Run Test/Idle (see Figure 9), and TAP2 (now linked) remains in Run Test/Idle (see Figure 9). On the next rising TCK edge, the test bus transitions to the Select DR Scan state, TAP2 transitions with the test bus to the Select DR Scan state, and TAP1 remains in the Run Test/Idle state.

Figure 11 shows a timing example wherein unlinked TAP2 becomes linked and linked TAP1 becomes unlinked while the test bus transitions from the UpdateDR state directly to the Select DR Scan state. The link change occurs on the falling edge of the TCK in the UpdateDR state with EN1 of TAP1 going low and EN2 of TAP2 going high. On the next rising TCK edge, the test bus transitions into the Select DR Scan state, TAP1 is forced to transition to Run Test/Idle (see Figure 9), and TAP2 transitions with the test bus from Run Test/Idle to the Select DR Scan state (see Figure 9). On the next rising TCK edge, the test bus transitions to the Select IR Scan state, TAP2 transitions with the test bus to the Select IR Scan state, and TAP1 remains in the Run Test/Idle state.

After completing all TAP accesses, the test bus can transition to the Test Logic Reset state. TAP(s) currently linked to the test bus will follow it into the Test Logic Reset state. TAP(s) not linked to the test bus (i.e. TAPs unlinked and left in Run Test/Idle state) will be forced to the Test Logic Reset state by the Reset output from the TLM TAP Controller 31 (Figures 3 and 4) which always follows the test bus transitions and will output the Reset signal to all TAPs (see Figures 2-5) when the test bus enters the Test Logic Reset state.

To provide flexibility in using TLM 21 or TLM 51 to enable and disable TAPs within an IC, the TLMs should preferably be selectable during some or all of the instructions defined for each TAP. For example, the 1149.1 standard defines the following list of required and optional TAP instructions: Bypass, Extest, Sample/Preload, Intest, RunBist, Clamp, Highz, Idcode, and Usercode. During Bypass, Sample/Preload, Idcode, and Usercode instructions, the functional circuit associated with the TAP remains in its normal operation mode. During Extest, Intest, RunBist, Clamp, and Highz instructions, the functional circuit associated with the TAP is disabled from its normal operation mode. Users of the 1149.1 standard may define and add instructions to achieve customized test operations, such as internal scan, emulation, or on-line BIST.

The flexibility of using the TLMs is enhanced if each of the aforementioned conventional instructions is replaced by a pair of instructions according to the present invention, which pair of instructions determine whether or not the TLM is selected. For example, the conventional Extest instruction selects the boundary scan register to scan data between the IC's TDI and TDO pins, but does not at all comprehend the select output SEL4 shown in Figure 7. Accordingly, one instruction of the Extest replacement pair would (1) select the boundary scan register like the conventional Extest instruction, (2) deactivate the SEL4 output to deselect the TLM, and (3) otherwise affect the IC the same as the conventional Extest instruction. Another instruction of the Extest replacement pair would (1) deselect the boundary scan register, (2) activate SEL4 to select TLM for scanning, and (3) otherwise affect the IC the same as the conventional Extest instruction.

One advantage is that TLM can be operated to disable one TAP and enable another while maintaining the effect of the current instruction on the functional circuit associated with the TAP being disabled. For example, in Figures 2 and 5 it may be desirable to disable the IC's I/O while performing a test or emulation operation on MM1. To do this, TAP1 would be enabled and scanned with a Highz instruction version that selects the TLM and deselects the bypass register but otherwise affects the IC the same as the conventional Highz instruction, which will disable the IC's I/O. Next, a data register scan to the TLM disables scan access to TAP1 and enables scan access to TAP2 to enable the desired test or emulation operation on MM1. While test or emulation occurs on MM1, the Highz instruction version, left in effect in TAP1, keeps the IC's I/O disabled. Other 1149.1 instructions or user defined instructions can be similarly replaced by a first instruction that deselects TLM and selects a data register within the TAP and a second instruction that deselects the TAP data register and selects the external TLM, both replacement instructions otherwise affecting the IC the same as the corresponding conventional instruction.

Example Figures 16-17A illustrate the above-

described replacement of a given conventional instruction with a pair of replacement instructions which select or deselect TLM. Figure 16 illustrates various functions which are controlled by the instruction register in the conventional IEEE STD 1149.1 architecture of Figure 12. In Figure 16, an instruction is shifted into the shift register 162, and shift register bits SRB3, SRB2, and SRB1 (i.e. the instruction) are then decoded by decode logic 165. The output of the decode logic is loaded into an update register 167 whose outputs control various functions in the test architecture. In the Figure 16 example, six signals are output from the update register to control the various functions. Signal BR enables the bypass register to scan data therethrough, signal BSR enables the boundary scan register (BSR) to scan data therethrough, the MODE signal applied to BSR determines whether BSR is in a test mode for handling test data or a transparent mode for passing normal functional signals therethrough, the HIGHZ signal can disable the output buffers 163 of the integrated circuit or core megamodule, the BENA signal is a Bist enable signal for enabling Bist operations, and the REGSEL signal controls multiplexer 161 to determine which data register (in this example the bypass register or BSR) will be connected to the input of multiplexer 121, which in turn determines whether a data register or the instruction register will be scanned.

Figure 16A shows conventional instructions for use with the conventional architecture of Figure 16. Each of the instructions is decoded to produce the indicated logic levels on the six control signals of Figure 16. For example, the HighZ instruction enables the bypass register for scanning (BR=1) disables BSR for scanning (signal BSR=0), places BSR in the transparent mode (MODE=0), disables the output buffers 163 (HIGHZ=1), disables Bist (BENA=0), and selects the bypass register at multiplexer 161 (REGSEL=0). As another example, the conventional Extest instruction disables the bypass register for scanning (BR=0), enables BSR for scanning (signal BSR=1), places BSR in the test mode (MODE=1), enables the output buffers 163 (HIGHZ=0), disables Bist (BENA=0), and selects BSR at multiplexer 161 (REGSEL=1).

Exemplary Figure 17 illustrates in more detail the instruction register control within TAP4 of Figure 7 according to the present invention. The remaining TAPs 1-3 can be designed analogously. The update register 175 of Figure 17 outputs the six control signals of Figure 16 plus the signal SEL4 to select TLM. The shift register 171 of Figure 17 has an additional shift register bit SRB4 because the six example instructions from Figure 16A require twelve replacement instructions according to the present invention as shown in Figure 17A. The additional bit SRB4 is thus needed to uniquely encode the twelve instructions of Figure 17A.

Referring to Figure 17A the replacement pair for the conventional HighZ instruction is seen at the third and ninth entries of the table of Figure 17A. More specifi-

cally, the HighZ instruction with TLM not selected is decoded at 173 (see Figure 17) to output the same logic levels as the conventional HighZ instruction and additionally to output a logic 0 on the SEL4 output in order to ensure that TLM is not selected. The decoded output of the HighZ instruction with TLM selected is the same as the decoded output of the HighZ instruction with TLM not selected, except BR=0 and SEL4=1 to ensure that TLM is selected and the bypass register is deselected. Similarly, the decoded output of the Extest instruction with TLM not selected includes the same six logic levels as the conventional Extest instruction, plus a logic 0 on SEL4 to ensure that TLM is not selected. The decoded output of the Extest instruction with TLM selected is the same as the decoded output of Extest with TLM not selected, except the BSR signal is at logic 0 to deselect BSR, and SEL4=1 to select TLM. Thus, the above-described instruction pairs and the other instruction pairs shown in Figure 17A permit selection of either TLM or an internal data register (such as the bypass register or BSR) for scanning, but both instructions of each instruction pair otherwise provide the identical control signals provided by the corresponding conventional instructions illustrated in Figure 16A. Thus, the instruction pairs of Figure 17A permit TAP4 to select for scanning either the external data path in TLM, or an internal data register such as the bypass register or BSR, while otherwise outputting control signals which are identical to those associated with the corresponding conventional instructions of Figure 16A.

Execution of RunBist operations is improved by using the RunBist replacement instructions. The conventional RunBist instruction initiates a Bist (Built-In-Self-Test) operation when the TAP enters Run Test/Idle, but the conventional RunBist instruction selects a data register inside the TAP (boundary scan register in Figures 16-17) for scanning. A first TAP can be enabled and scanned with the replacement RunBist instruction that selects the TLM and deselects the boundary scan register. After scanning the TLM to enable a second TAP, the first TAP gets disabled and automatically transitions into the Run Test/Idle state (Figures 9-11) where the replacement RunBist instruction takes effect to initiate the Bist operation. While the first TAP is executing the Bist operation in Run Test/Idle, the second TAP can be scanned with the aforementioned replacement RunBist instruction that selects the TLM and deselects the boundary scan register. Scanning the TLM to enable a third TAP will force the second TAP to the Run Test/Idle state where the replacement RunBist instruction takes effect to initiate a Bist operation. This scheme can continue to sequentially select TAPs and initiate Bist testing in as many TAPs as desired. Thus, BIST operations in the selected megamodules can occur in time overlapping fashion rather than purely sequentially. This of course provides time savings.

To obtain the Bist result from BSR of Figure 17, TAP4 can be enabled via TLM, and then loaded with the

replacement RunBist instruction that deselects TLM and selects BSR. With BSR selected, the Bist result can be scanned out of BSR by a data register scan operation.

The architecture of Figure 5 can also execute the above procedure to initiate multiple RunBist operations, or it could simply enable/link all or selected ones of the TAPs together, scan in a conventional RunBist instruction to each, then enter Run Test/Idle to concurrently execute the RunBist instructions. After linking a first group of TAPs together in Figure 5, each of them can be loaded with the replacement RunBist instruction that selects TLM 51, and thereafter the first group can be unlinked via TLM 51 so the first group can execute Bist operations in Run Test/Idle while TLM 51 is linking a second group of TAPs to repeat the same procedure. So while the Figure 2 architecture allows for enabling a TAP, loading RunBist, and then disabling the TAP to effect Bist operations in a megamodule, the Figure 5 architecture allows enabling/linking a group of TAPs, loading RunBist, and then disabling/unlinking the group of TAPs to effect concurrent Bist operations in a group of megamodules. The capability of sequentially selecting groups of TAPs so that each group performs Bist operations concurrently within the group and in time-overlapping fashion relative to other groups provides additional flexibility to choose the most time-efficient approach for a given IC's megamodule layout.

Although providing a replacement instruction pair for each instruction will allow for leaving any instruction in effect after a TAP has been disabled, a single instruction can be defined to select the TLM if desired. When using a single TLM select instruction, the TAP cannot maintain the effect of a specific instruction on the IC when the TLM is accessed.

The TAP linking approach described herein could be accomplished on a substrate (e.g. multichip module or board) comprising individual circuits (e.g. die or IC), each having a TAP with externally accessible select and enable signals corresponding to SEL1-4 and EN1-4. Also required on the substrate would be a TLM circuit (e.g. die or IC). Further, to support the plural TAP linking scheme of Figure 5, multiplexer circuits (e.g. die or IC) would be required on the TDI inputs of some or all of the TAP'ed circuits.

Although exemplary embodiments of the present invention are described above, this description does not limit the scope of the invention, which can be practiced in a variety of embodiments.

50 Claims

1. An integrated circuit comprising:

55 a test bus;
a plurality of target circuits; and
a plurality of test interfaces coupled between
said test bus and the respective target circuits,

said test interface having a register select output for selecting a register for performing a data transfer operation.

2. A method of using a plurality of test interfaces, said interfaces being coupled between a test bus and respective one of a plurality of target circuits to provide access to a register comprising:

receiving register select signals from respective test interfaces;

responding to a first of the register select signals including selecting the register to perform a data transfer operation; and

responding to a second of the register select signals including selecting the register to perform a data transfer operation.

3. A scan test architecture comprising:

a scan controller;

a first scannable test data register arranged to be coupled to said scan controller for scanning data in response to a first scan control signal generated by said scan controller;

a second scannable test data register arranged to be coupled to a second scan control signal for scanning data in response to said second scan control signal, said second scan control signal being generated independently of said scan controller; and

a scannable control circuit having an output for selecting said first scannable register for scanning and also for selecting said second scannable register for scanning.

4. A method of controlling first and second scannable test data registers comprising:

using a scan controller to generate a first scan control signal;

using the first scan control signal to control scanning of the first register;

generating a second scan control signal independently of the scan controller;

using the second scan control signal to control scanning of the second register;

using a scannable control circuit to select the first register for scanning; and

using the scannable control circuit to select the second register for scanning.

5. A method of testing first and second target circuits via first and second test interfaces coupled between a test bus and a respective one of a plurality of target circuits comprising:

preparing to test the first target circuit, includ-

ing accessing the first test interface via the test bus;

thereafter, testing the first target circuit in response to the first test interface; and

during said step of testing said first target circuit, preparing to test the second target circuit, including accessing the second test interface via the test bus.

6. An electrical circuit, comprising:

a test bus;

a target circuit;

a test interface arranged to be coupled between said test bus and said target circuit, said test interface including a first state machine operable to assume a plurality of states in response to signals received via said test bus;

a second state machine coupled to said test bus and to said first state machine, said second state machine operable to assume a plurality of states in response to signals received via said test bus; and

said first state machine operable to assume a predetermined one of said states associated therewith in response to an advancement of said second state machine, through a predetermined sequence of said states associated therewith.

7. A method of using a first state machine to control a test interface coupled between a test bus and a target circuit and which includes a second state machine, comprising:

advancing the first state machine through a predetermined sequence of states in response to signals received via the test bus; and

causing the second state machine to assume a predetermined state in response to the advancement of the first state machine through the predetermined sequence of states.

8. An electrical circuit, comprising:

test bus;

plurality of target circuits;

a plurality of test interfaces arranged to be coupled to said test bus for simultaneous communication therewith, said test interfaces arranged to be coupled between said test bus and respective target circuits, each said test interface including an enable input indicative of when said test interface is enabled for communication with said test bus and also indicative of when said test interface is disabled from communication with said test bus.

9. A method of accessing a plurality of test interfaces, the test interfaces coupled to a test bus for simultaneous communication therewith, the test interfaces also being coupled to respective target circuits, which method comprising:

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enabling a first of the test interfaces for communication with the test bus;
communicating test information between the test bus and the first test interface; and
disabling a second of the test interfaces from communication with the test bus while the first test interface is communicating with the test bus.

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10. An integrated circuit comprising:

a test bus;
a target circuit;
a test interface for coupling between said test bus and said target circuit; said test interface including:

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a scan controller;
a first scannable test data register for coupling to said scan controller for scanning data in response to a first scan control signal generated by said scan controller;
a scannable control circuit responsive to a first control code scanned into said first scannable test data register for selecting said first test data register to be scanned and for providing a control signal to said target circuit; and
a second scannable test data register coupled to a second scan control signal for scanning data in response to said second scan control signal, said second scan control signal being generated independently of said scan controller, said scannable control circuit being responsive to a second control code scanned thereinto for selecting said second test data register to be scanned and for providing said control signal to said target circuit.

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said state machine arranged to receive an override signal; and

said state machine, when in said first state, responsive to said override said signal to ignore said predetermined condition of said test bus and assume a state other than said second state.

12. A method of operating a test interface coupled between a target circuit and a test bus and which includes a state machine comprising:

responding to a predetermined condition of the test bus when the state machine is in a first state, including causing the state machine to advance from the first state to a second state; indicating that an override is desired; and with the state machine in the first state, responding to the override indication, including ignoring the predetermined condition of the test bus and causing the state machine to assume a state other than said second state.

11. An integrated circuit, comprising:

test bus;
target circuit;
a test interface arranged to be coupled between said test bus and said target circuit, said test interface including a state machine which, when in a first state, is normally responsive to a predetermined condition of said test bus to advance from said first state to a second state according to a predetermined state diagram associated with said state machine;

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Figure 1
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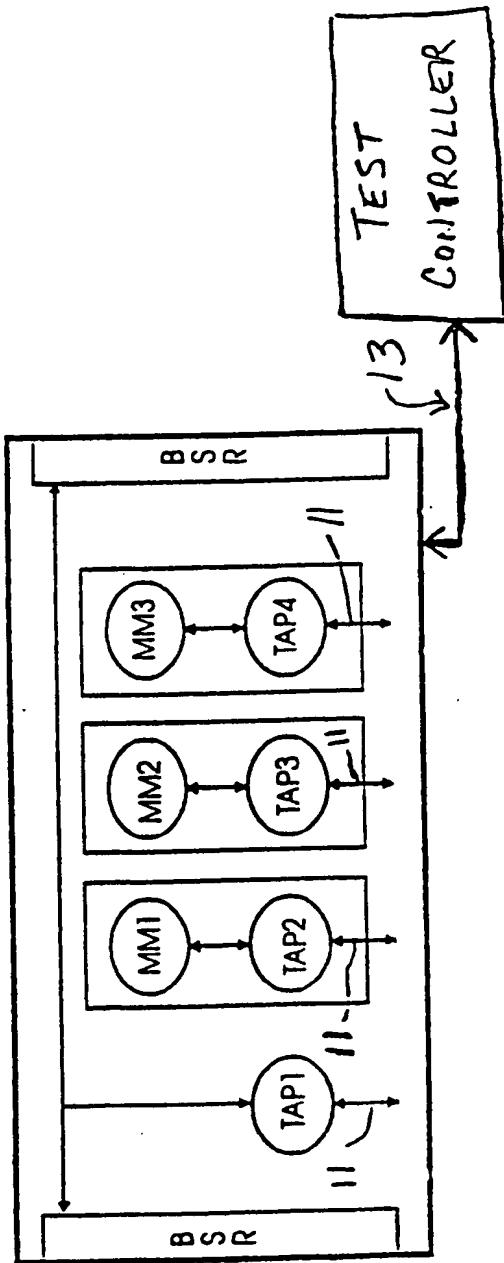


Figure 2

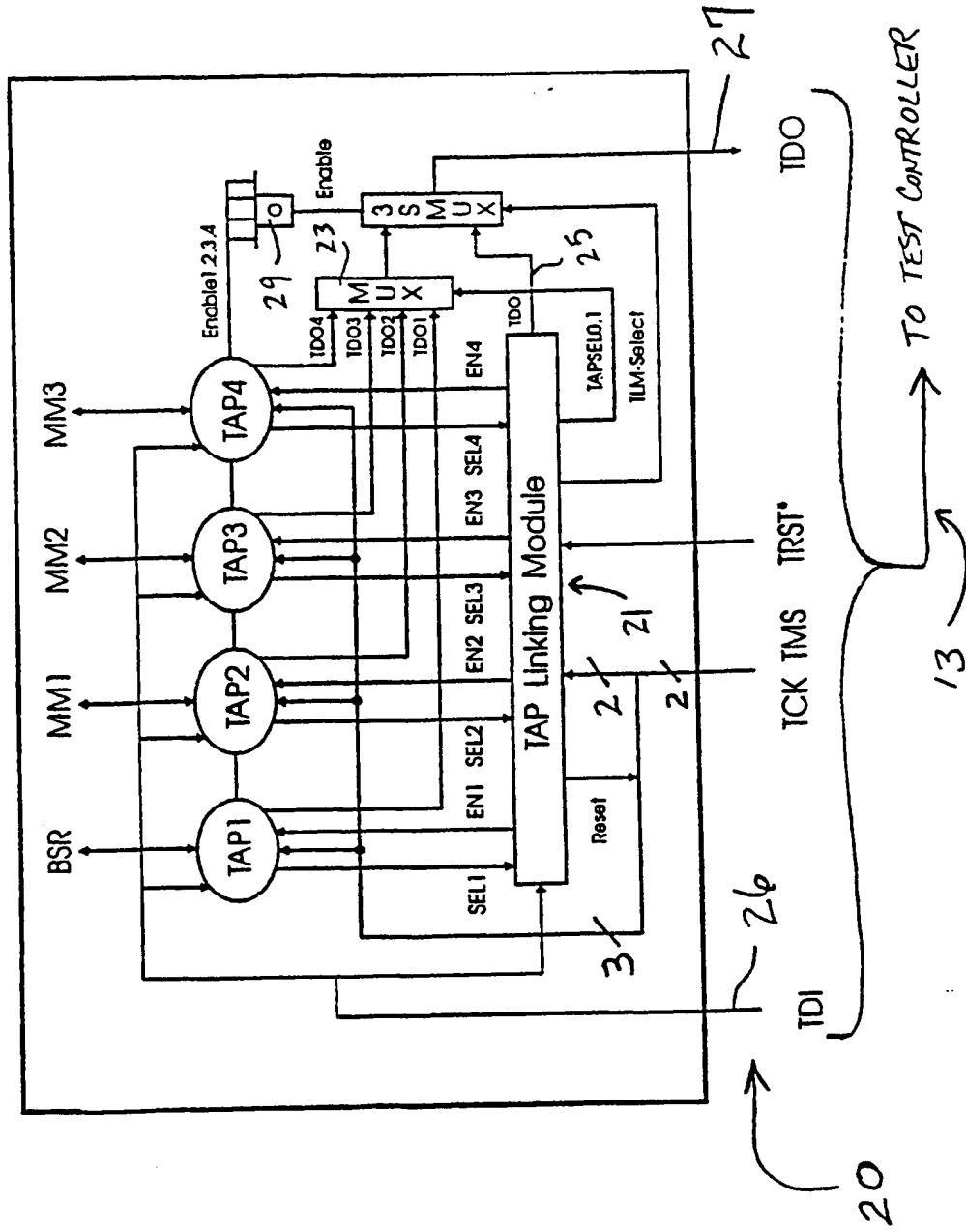


Figure 3

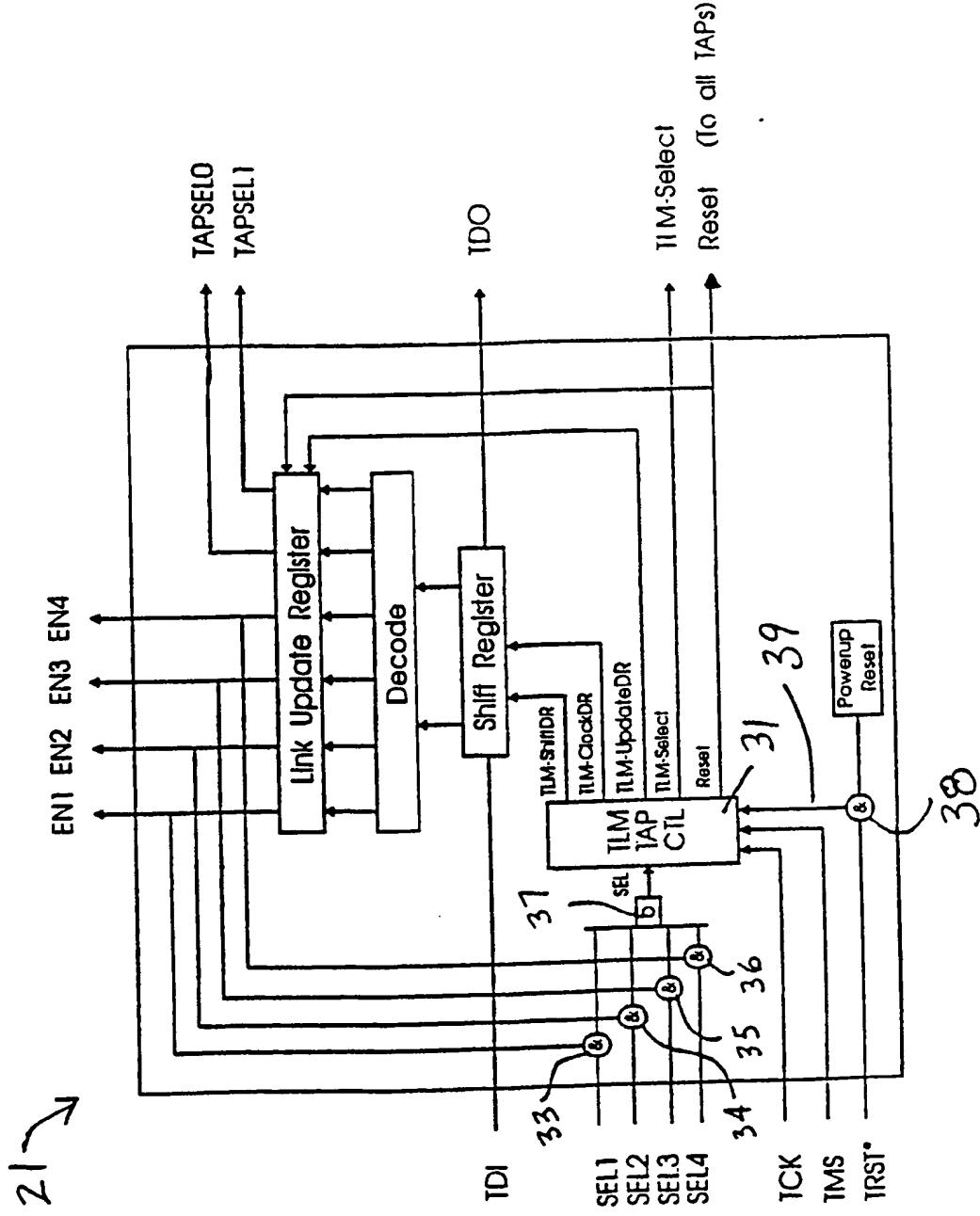


Figure 4

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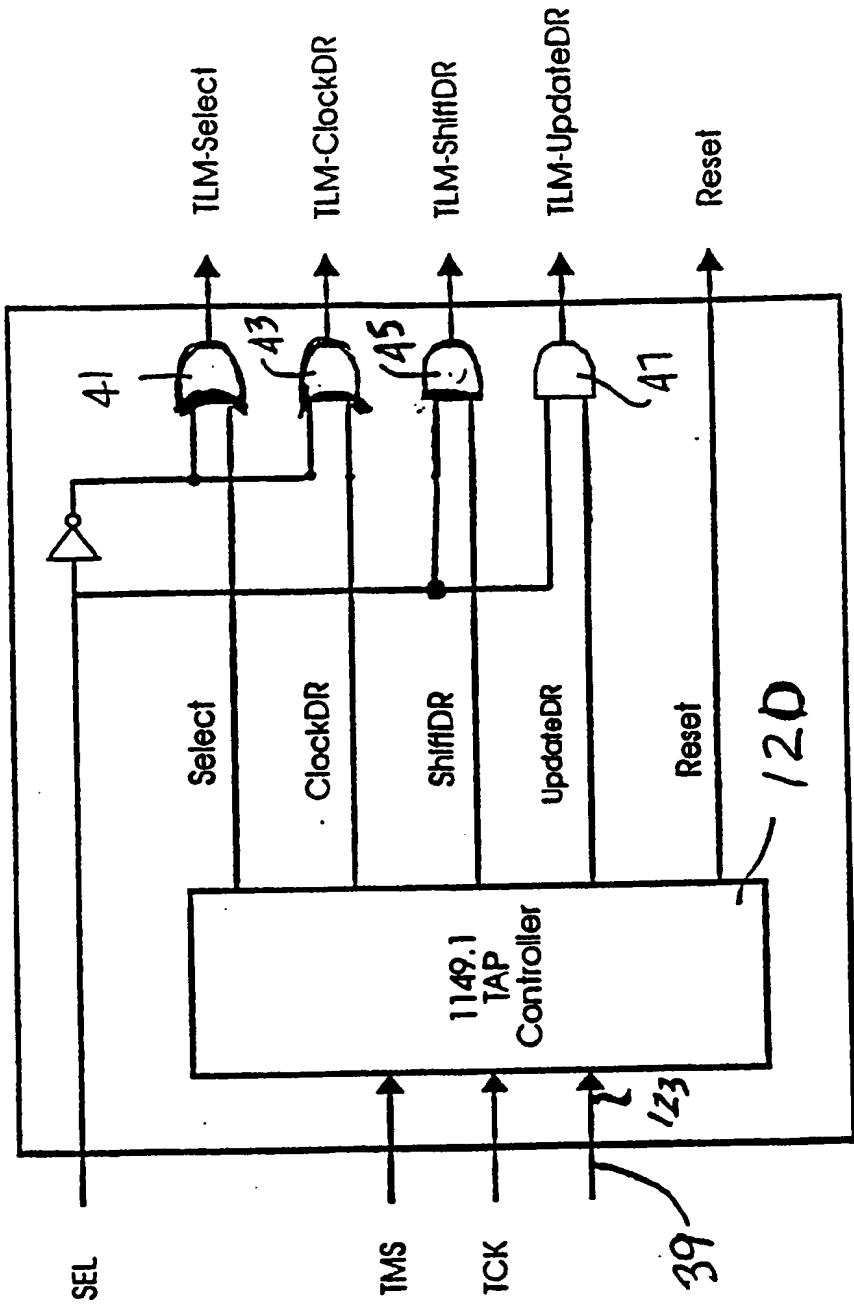


Figure 5

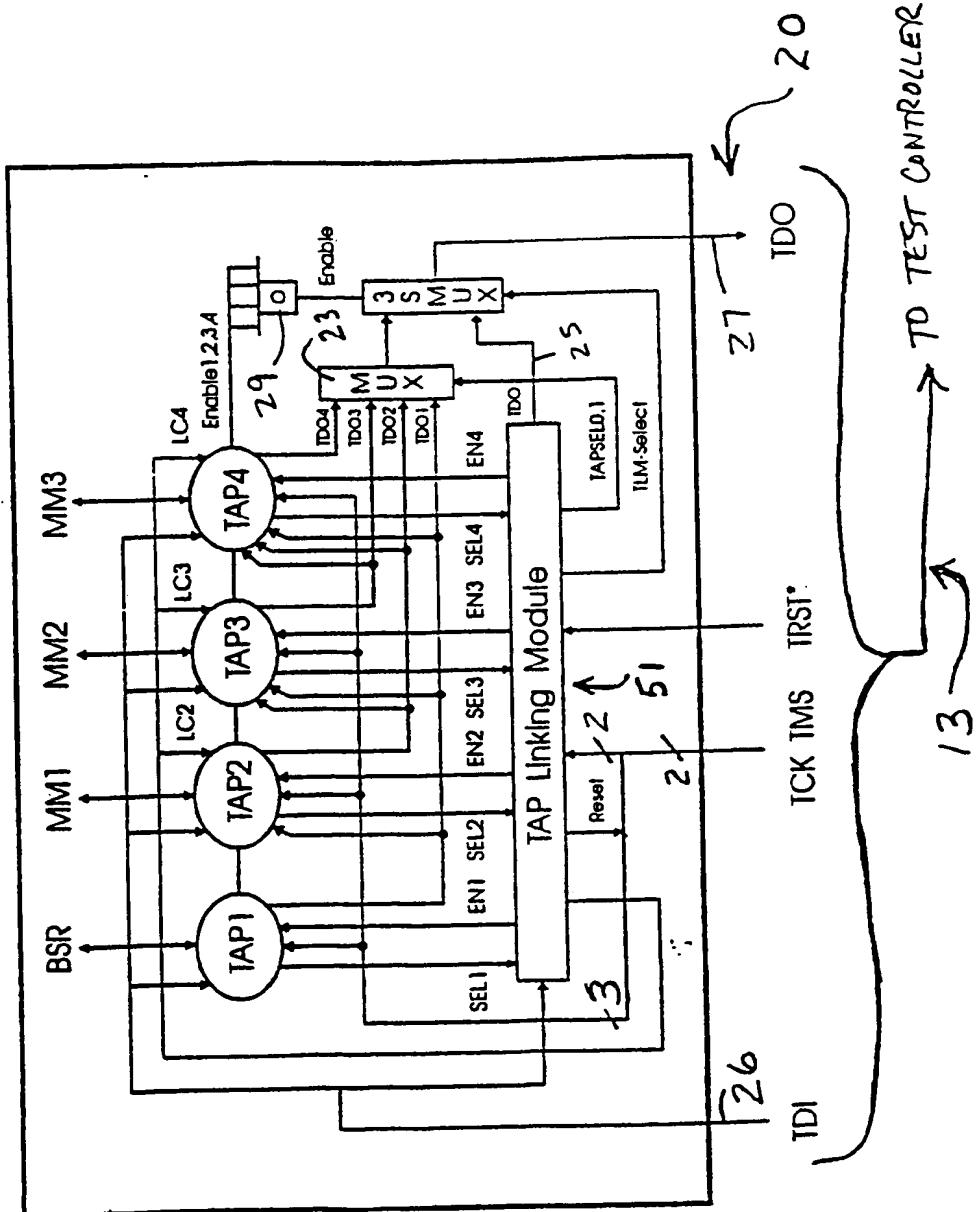


Figure 6

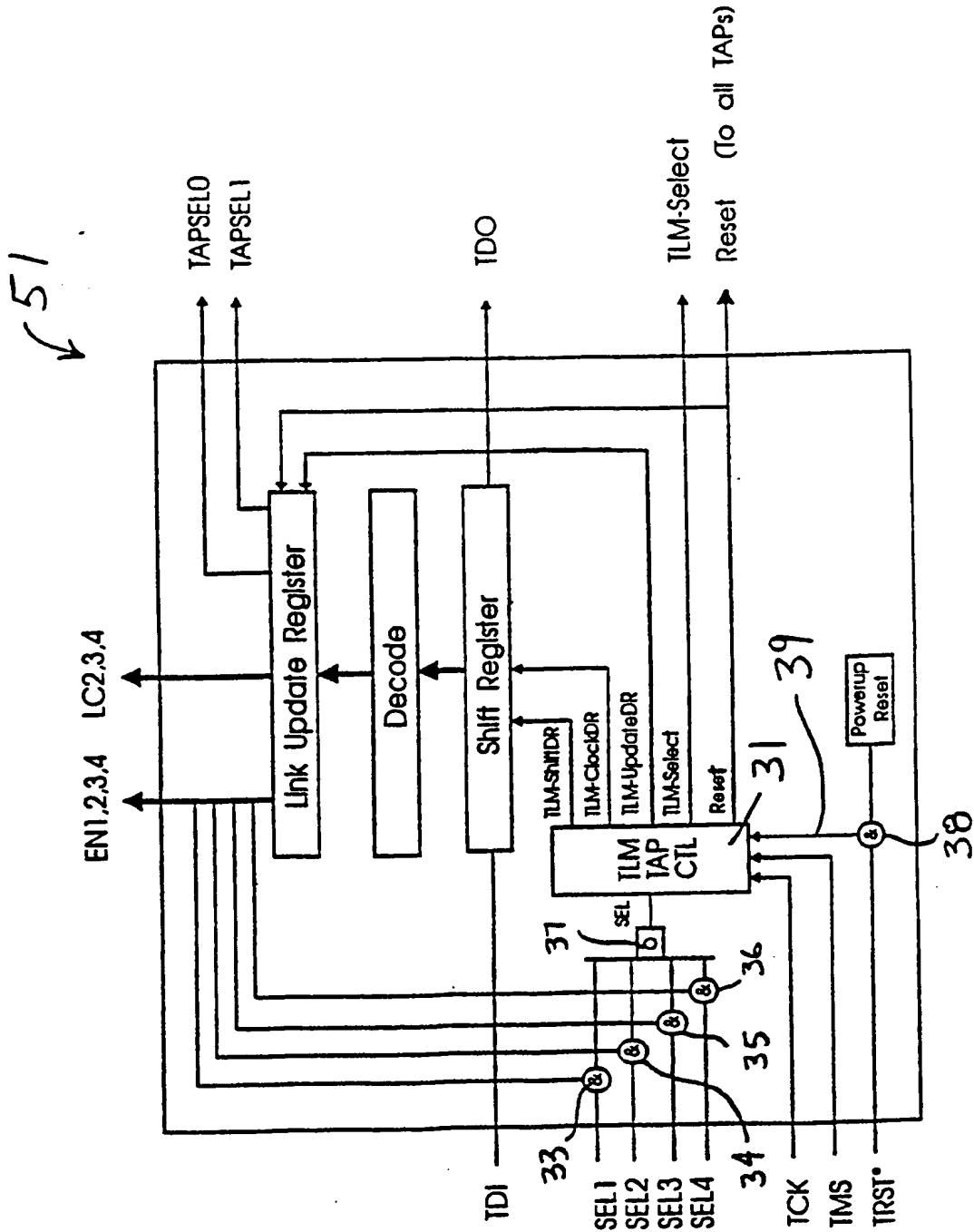


Figure 7

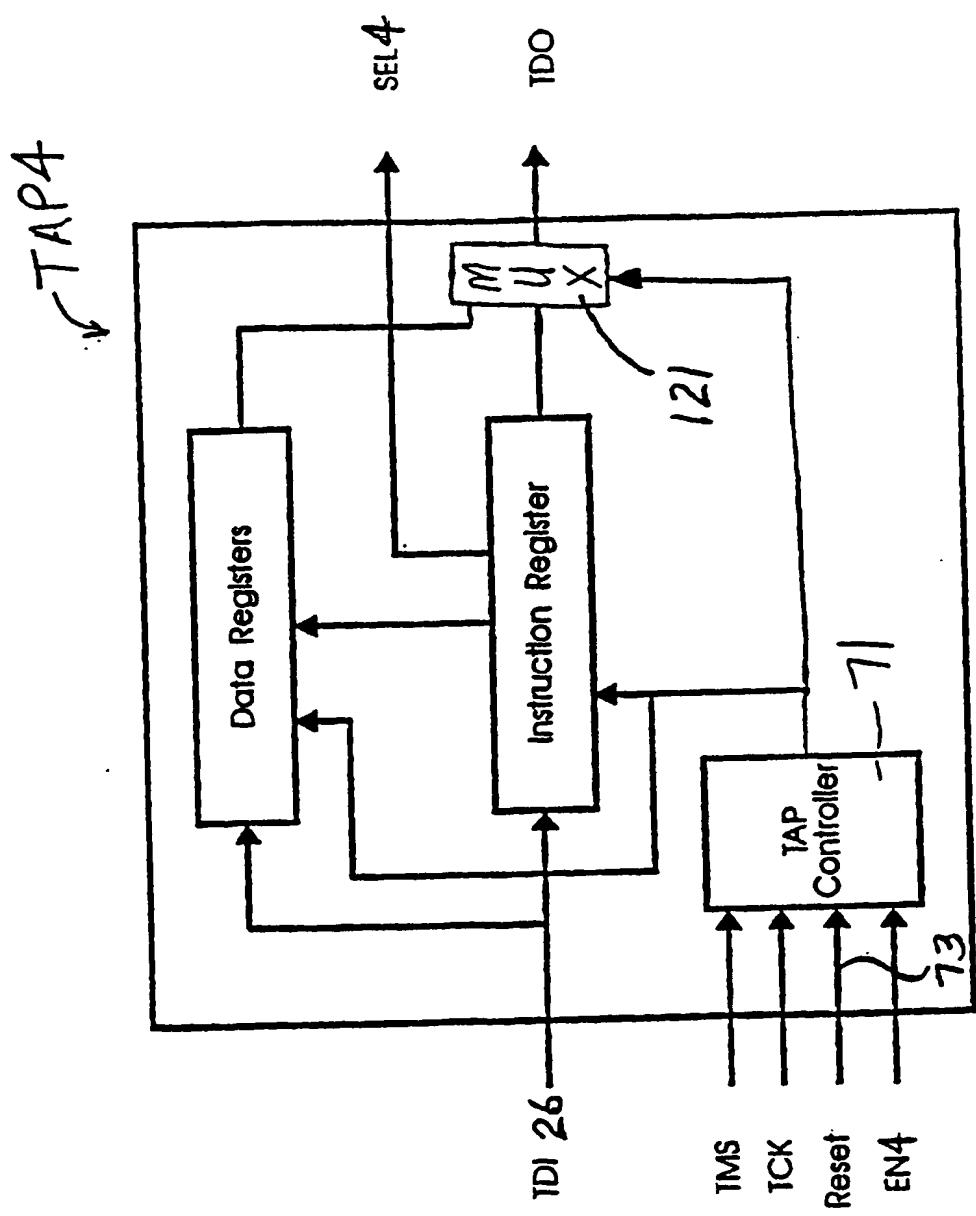


Figure 8

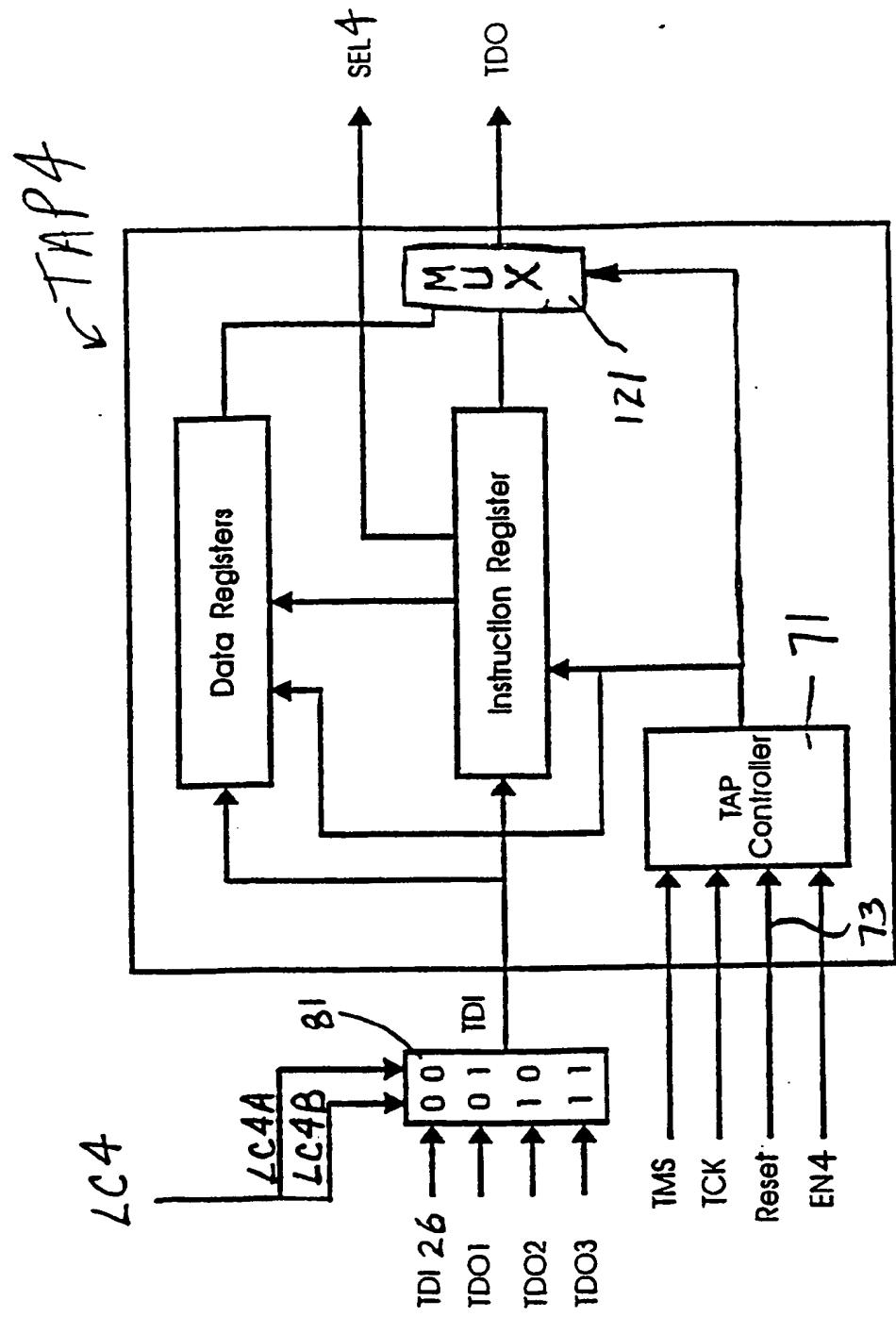


Figure 9

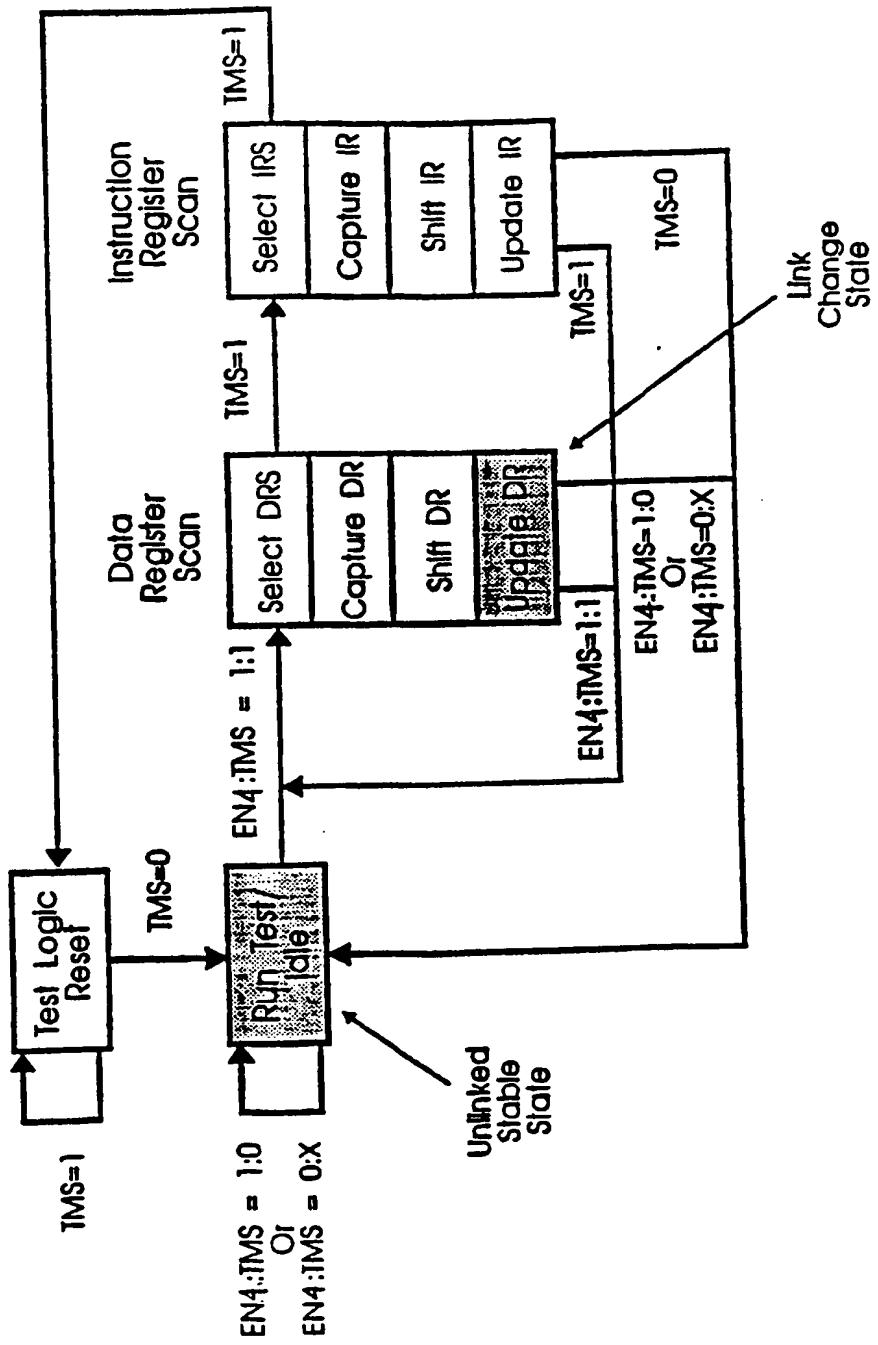


Figure 9A

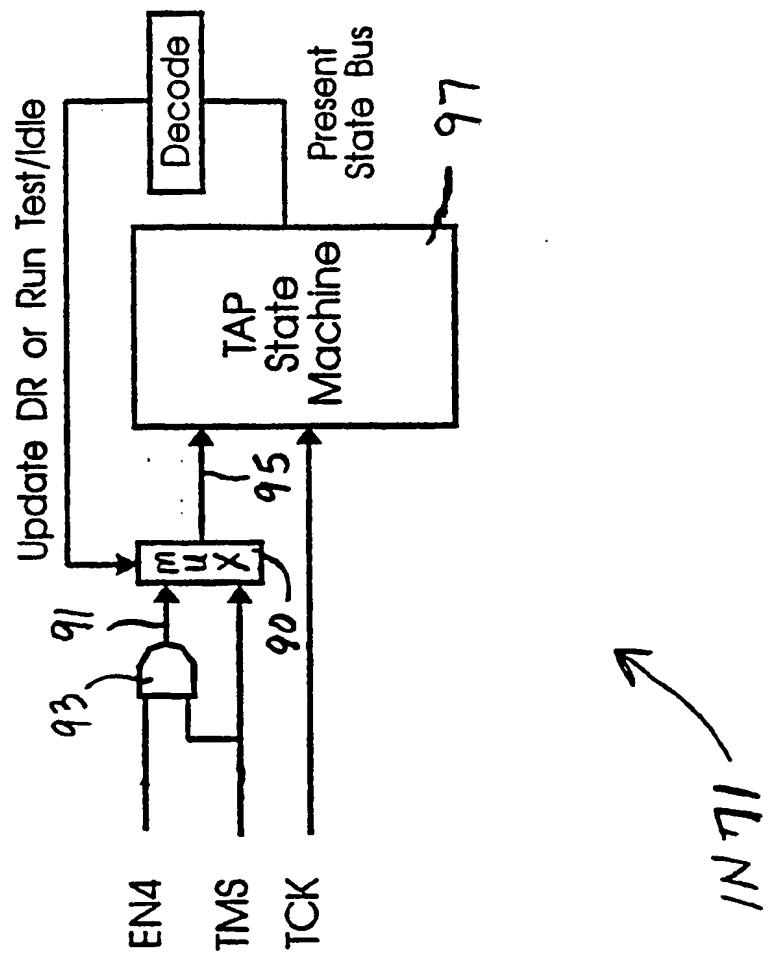


Figure 10

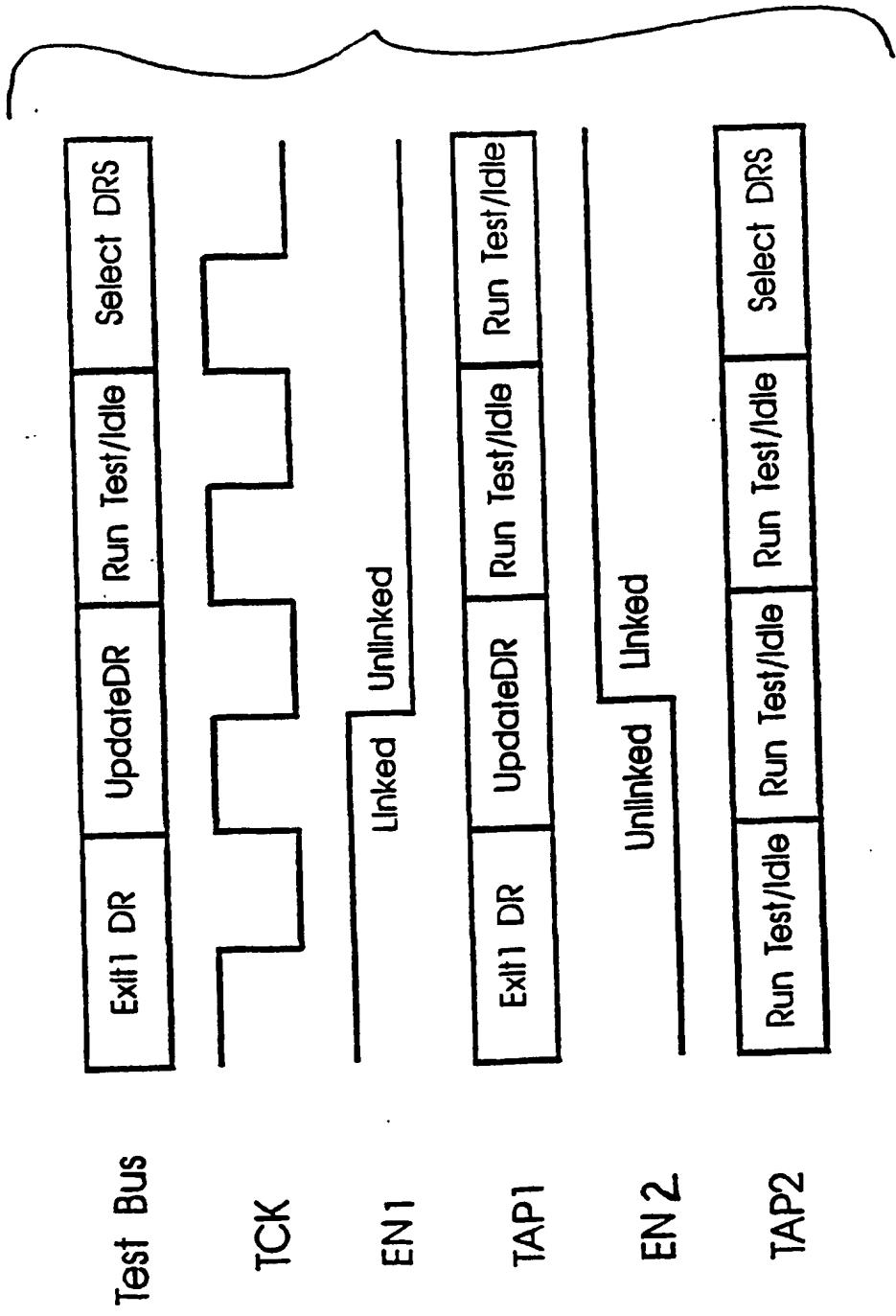
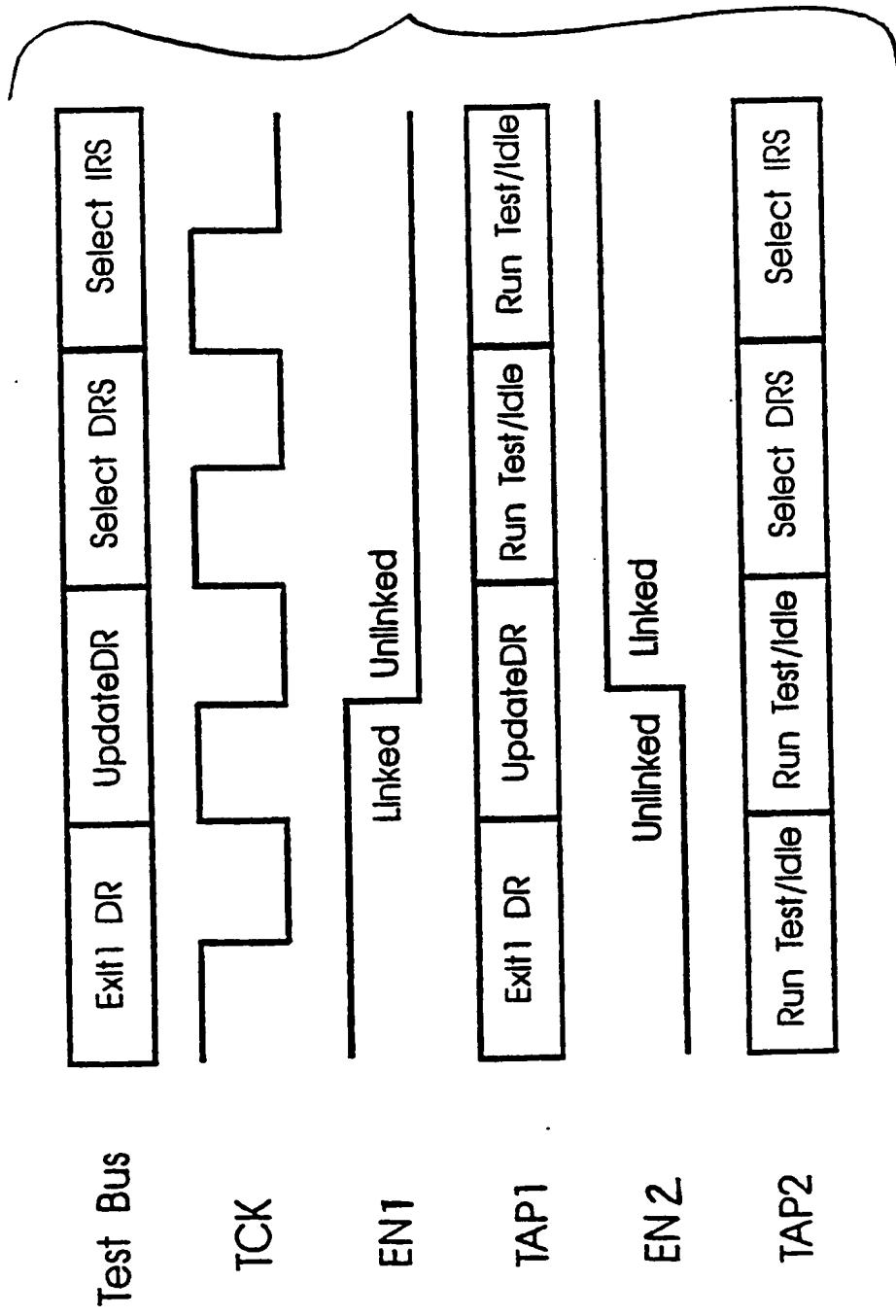
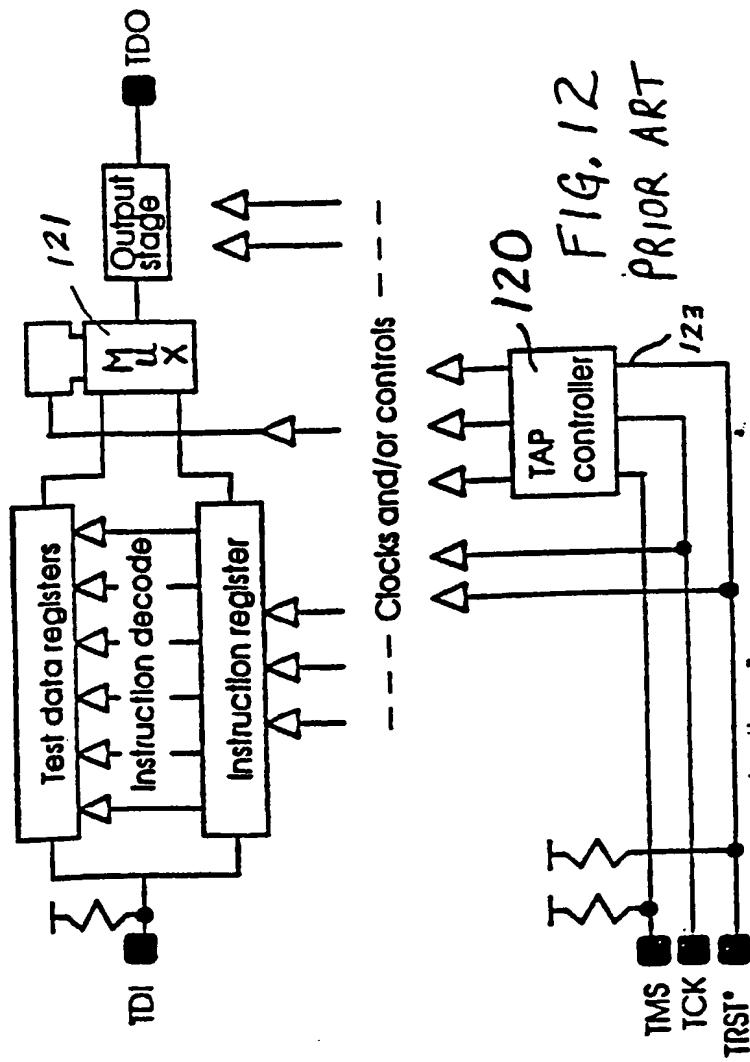


Figure 11





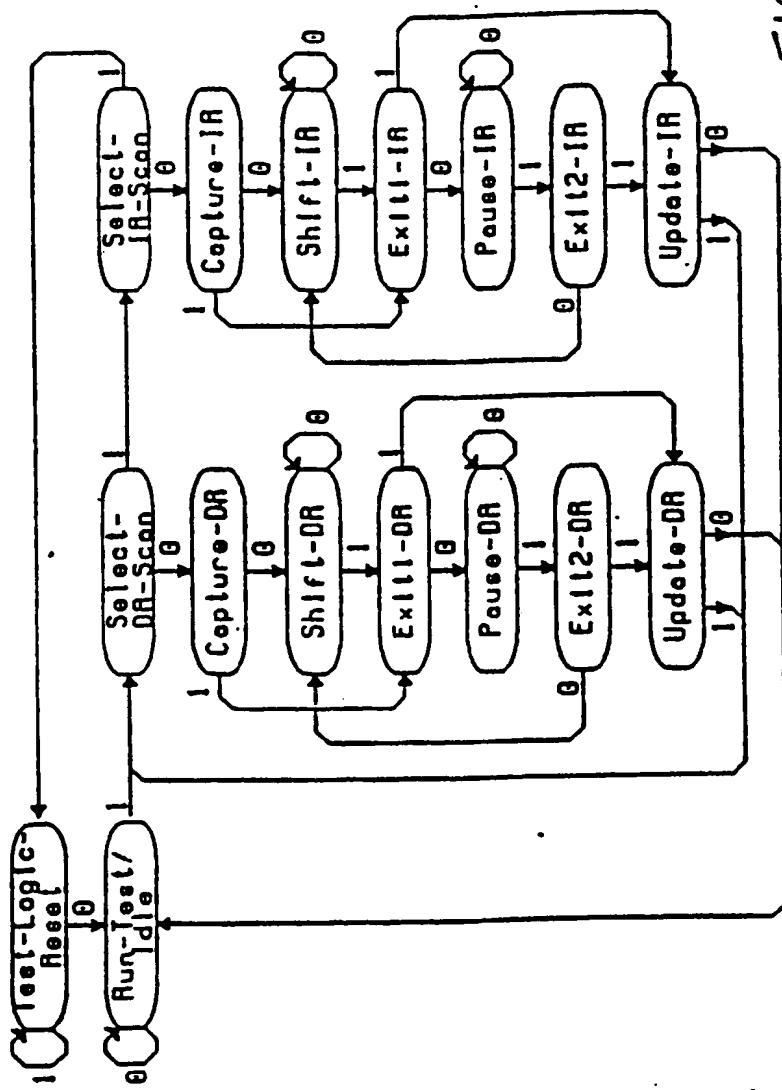


FIG. 14

PRIOR ART

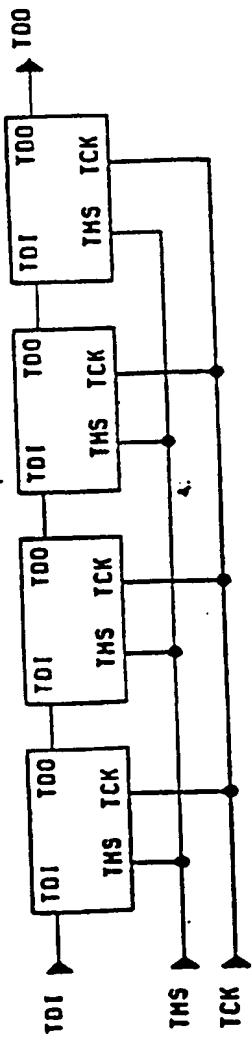


FIG. 13
Priority list

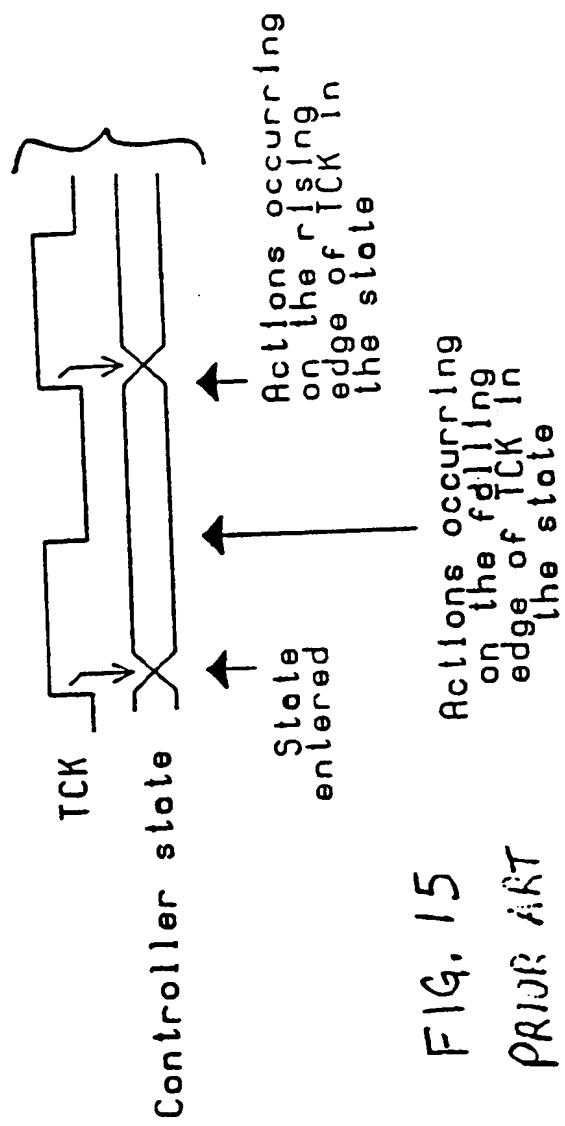


FIG. 15
Priority list

Figure 16
PRIOR ART

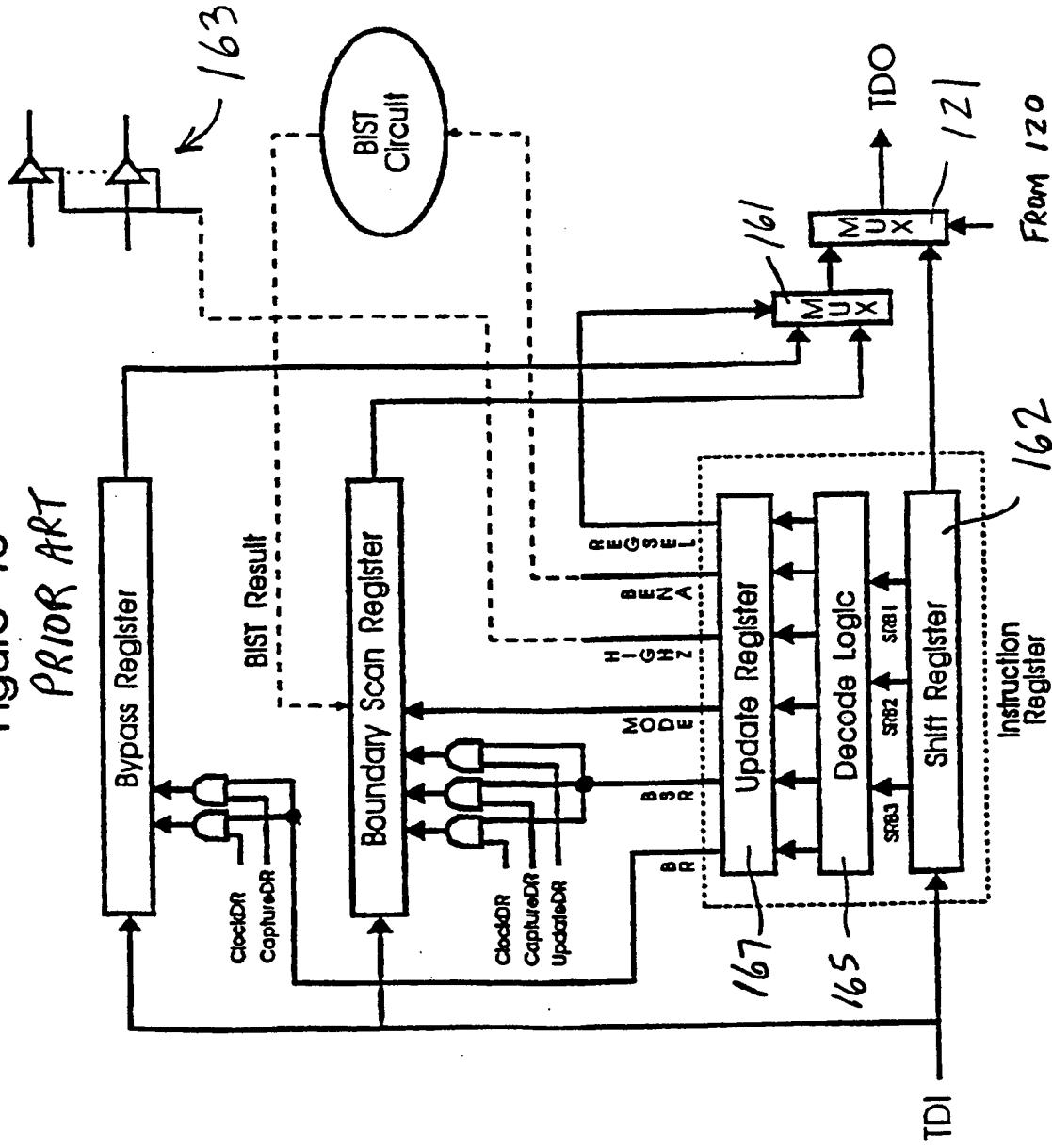


Figure 16A
PRIOR ART

	S	S	S	R	R	R	B	B	B	R	R	R	B	S	D	O	H	G	E	R	
Instruction	3	2	1	3	2	1	3	2	1	3	2	1	3	2	1	3	2	1	3	2	1
Bypass	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Sample	0	0	1	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0
HighZ	0	1	0	1	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0
Clamp	0	1	1	1	0	1	1	0	1	0	1	0	0	0	0	0	1	1	0	1	1
RunBIST	1	0	0	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1
Extest	1	1	1	0	1	1	0	1	1	0	1	1	0	0	1	0	0	1	0	0	1

Figure 17

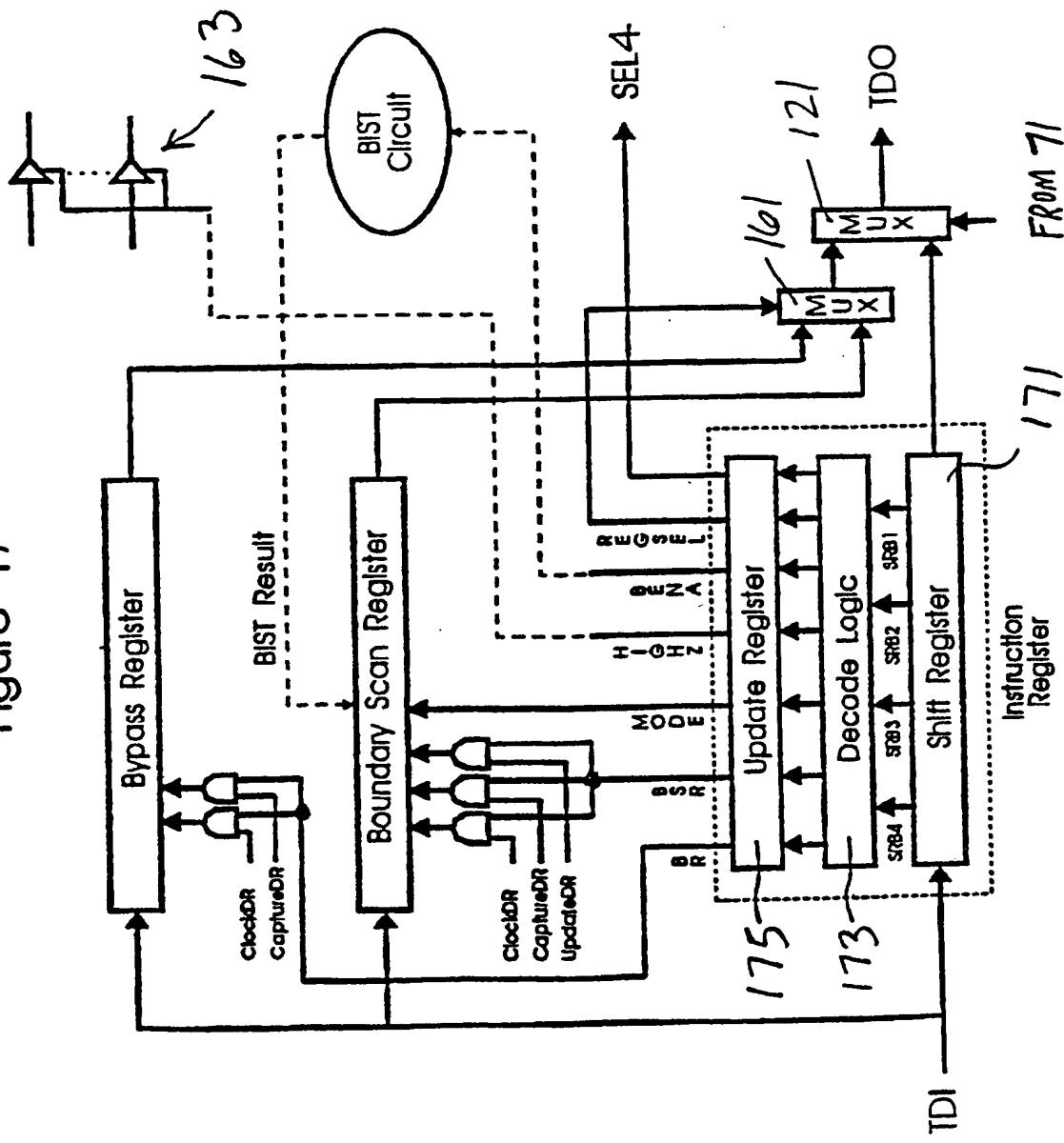


Figure 17A

Instruction	S R	S B	S 2	R B	R B	R 1	B R	B R	G D	E H	E Z	E A	E L	R M	E O	E D	G E	E N	E H	G A	S L
	4																				
Bypass TLM not Selected	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Sample TLM not Selected	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
HighZ TLM not Selected	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
Clamp TLM not Selected	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
RunBist TLM not Selected	0	1	0	0	0	1	1	0	1	0	1	1	0	0	0	0	0	1	0	0	0
Exttest TLM not Selected	1	1	1	1	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0
Bypass TLM Selected	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Sample TLM Selected	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
HighZ TLM Selected	1	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	0
Clamp TLM Selected	1	0	1	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0
RunBist TLM Selected	1	1	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1
Exttest TLM Selected	1	1	0	1	0	0	0	1	0	0	1	0	0	1	1	1	1	1	1	1	1



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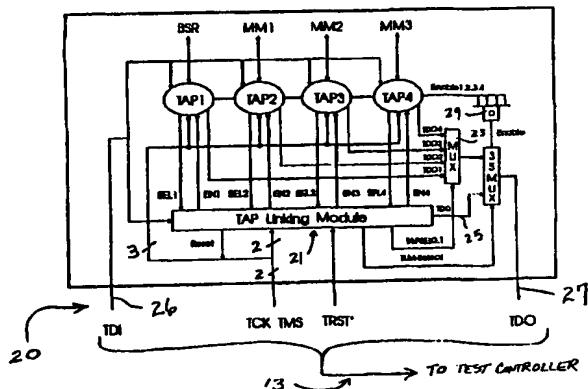
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(54) Method and device for testing integrated circuits

(57) A TAP linking module (21, 51) permits plural TAPs (TAPs 1-4) to be controlled and accessed from a test bus (13) via a single TAP interface (20).

Figure 2



EP 0 826 974 A3



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 11 4556

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.Cl.6)						
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim							
X	EP 0 661 551 A (AT & T CORP) 5 July 1995 * abstract; claims 1-6; figure 1 *	1-12	G01R31/3185						
A	BREUER M A ET AL: "A TEST AND MAINTENANCE CONTROLLER FOR A MODULE CONTAINING TESTABLE CHIPS" NEW FRONTIERS IN TESTING, WASHINGTON, SEPT. 12 - 14, 1988, no. CONF. 19, 12 September 1988, pages 502-513, XP000013167 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * the whole document *	1-12							
A	MAUNDER C: "A UNIVERSAL FRAMEWORK FOR MANAGED BUILT-IN TEST" PROCEEDINGS OF THE INTERNATIONAL TEST CONFERENCE, BALTIMORE, OCT. 17-21, 1993, 1 January 1993, pages 21-29, XP000437119 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS * the whole document *	1-12							
A	US 5 448 525 A (STURGES JAY) 5 September 1995 * abstract; claim 1; figure 6 *	1-12	G01R						
A	US 4 701 921 A (POWELL THEO J ET AL) 20 October 1987 * abstract; claims 1-3 *	1-12							
<p>The present search report has been drawn up for all claims</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">Place of search</td> <td style="width: 33%;">Date of completion of the search</td> <td style="width: 34%;">Examiner</td> </tr> <tr> <td>THE HAGUE</td> <td>24 February 1999</td> <td>Sarasua Garcia, L</td> </tr> </table> <p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>				Place of search	Date of completion of the search	Examiner	THE HAGUE	24 February 1999	Sarasua Garcia, L
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